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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,807	02/12/2004	Dae-Gunn Jei	678-1315	5842
66547 7590 10/03/2007 THE FARRELL LAW FIRM, P.C. 333 EARLE OVINGTON BOULEVARD SUITE 701 UNIONDALE, NY 11553			EXAMINER BROWN, VERNAL U	
			ART UNIT 2612	PAPER NUMBER
			MAIL DATE 10/03/2007	DELIVERY MODE PAPER

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/777,807
Filing Date: February 12, 2004
Appellant(s): JEI ET AL.

Paul J. Farrell

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/25/07 appealing from the Office action mailed 9/29/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

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20020080864	Kuttruff et al.	6-2002
6972662	Ohkawa et al.	12-2005
20040198233	Pratt et al.	10-2004
20050215280	Twitchell Jr.	9-2005
6172518	Jenkins, IV. et al.	1-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 5, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662.

Regarding claim 1, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L, L2) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040); a

processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate first and second clock for the receiving and transmission part of the RFID device (figure 2) and one skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2).

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor and a second clock generator connected to the first clock generator, the codec, and the modulator in Kuttruff et al. because this enables the RFID device to clock the receiving and transmitting section of the RFID device separately for facilitating the different transmission and reception rates.

Regarding claim 2, Kuttruff et al. teaches the processor extracts the RFID data from the memory portion (paragraph 040) in response to information indicating the approach of the RFID reader, provided from the detector, and delivers the extracted RFID data to the codec (paragraph 0036).

Regarding claim 5, Kuttruff et al. teaches a rectifier for rectifying a voltage detected from a signal received via the antenna and delivering the rectified voltage to the processor (paragraph 0052).

Regarding claim 14, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L, L2) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor (figure 2).

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor in Kuttruff et al. because this enables the RFID device to reliably capture the receive data.

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Regarding claim 15, Kuttruff et al. teaches a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040) and a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040).

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 and further in view of Pratt et al. 20040198233.

Regarding claims 3-4, Kuttruff et al. teaches the detector generating a signal to the processor (paragraph 0039) but is silent on teaching the detector includes an interrupt port to the processor. Pratt et al. in an art related RFID device teaches the signal detected by a detector circuit connected to the interrupt port of the processor for enabling the processor to enter in an active mode (paragraph 0045). Pratt et al. also teaches a frequency detector for detecting the received frequency (paragraph 0048).

It would have been obvious to one of ordinary skill in the art for the detector to include an interrupt port to the processor in Kuttruff et al. because this enables the processor to be transformed into an active mode upon detecting a received signal from the interrogator.

Claims 6-7 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 and further in view of Twitchell Jr. US Patent Application Publication 20050215280.

Regarding claim 6, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L,

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L2) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056). The claims do not recite that a single memory element stores the claimed data, merely that a memory portion stores the data. It is the examiner's position that multiple memory elements can make up a memory portion as claimed. Kuttruff et al. teaches a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. teaches a power block comprising rectifier and voltage regulator (figure 2). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator and is also silent on teaching the processor commands the power block to provide electric power to the RFID module. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate first and second clock for the receive and transmission part of the RFID device (figure 2) and one

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skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2). Ohkawa et al. is also silent on teaching the processor commands the power block to provides electric power to the RFID module. Twitchell Jr. in an art related tag system invention teaches a processor commanding the power block to supply power to the RFID device (paragraph 0065) in order to conserve power when the device is not in use.

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor and a second clock generator connected to the first clock generator, the codec, and the modulator and the processor commands the power block to provides electric power to the RFID module in Kuttruff et al. because this enables the RFID device to clock the receive and transmitting section of the RFID device separately for facilitating the different transmission and reception rates. The controlling of the power supply by the processor allows the conservation of the power supply.

Regarding claim 7, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L₁, L₂) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE

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connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. teaches a power block comprising rectifier and voltage regulator (figure 2). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion and is also silent on teaching the processor commands the power block to provide electric power to the RFID module. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor. Ohkawa et al. is also silent on teaching the processor commands the power block to provides electric power to the RFID module. Twitchell Jr. in an art related tag system invention teaches a processor commanding the power block to supply power to the RFID device (paragraph 0065) in order to conserve power when the device is not in use.

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor because this enables the RFID device to reliably capture the receive data and the controlling of the power supply by the processor allows the conservation of the power supply.

Regarding claim 16, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L, L2) for communicating with the RFID reader (paragraph 0031); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048).

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Kuttruff et al. teaches a power block comprising rectifier and voltage regulator (figure 2).

Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion and is also silent on teaching the processor commands the power block to provide electric power to the RFID module. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor. Ohkawa et al. is also silent on teaching the processor commands the power block to provides electric power to the RFID module. Twitchell Jr. in an art related tag system invention teaches a processor commanding the power block to supply power to the RFID device (paragraph 0065) in order to conserve power when the device is not in use.

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor because this enables the RFID device to reliably capture the receive data and the controlling of the power supply by the processor allows the conservation of the power supply.

Regarding claim 17, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the

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memory portion; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate of a first and second clock for the receive and transmission part of the RFID device (figure 2) and one skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2).

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor because this enables the RFID device to reliably capture the receive data.

Regarding claim 18, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L, L2) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. teaches a power block comprising rectifier and voltage regulator

(figure 2). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion and is also silent on teaching the processor commands the power block to provide electric power to the RFID module. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate of a first and second clock for the receive and transmission part of the RFID device (figure 2) and one skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2). Ohkawa et al. is also silent on teaching the processor commands the power block to provides electric power to the RFID module. Twitchell Jr. in an art related tag system invention teaches a processor commanding the power block to supply power to the RFID device (paragraph 0065) in order to conserve power when the device is not in use.

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor because this enables the RFID device to reliably capture the receive data and the controlling of the power supply by the processor allows the conservation of the power supply.

Regarding claim 19, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate of a first and second clock for the receive and transmission part of the RFID device (figure 2) and one skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2).

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor because this enables the RFID device to reliably capture the receive data

Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 in view of Twitchell Jr. US Patent Application Publication 20050215280 and further in view of Jenkins, IV. et al. US Patent 6172518.

Regarding claim 8, Kuttruff et al. in view of Ohkawa et al. in view of Twitchell Jr. teaches the use of a processor to control the input power to the RFID module (see response to claim 7) but is silent on teaching the processor commands the power block using an enable pin. Jenkins, IV. Et al. teaches the conventional practice of using a power enable pin on a module to control the supply of power to the module (col. 2 lines 37-50) in order to conserve on the power supply.

It would have been obvious to one of ordinary skill in the art to command the power block using an enable pin because this provides an effective means of controlling the power supply base on external condition to the module in order to conserve on the power consumption.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 in view of Twitchell Jr. US Patent Application Publication 20050215280 and further in view of Appellant's Admitted prior art.

Regarding claim 9, Kuttruff et al. teaches a detector DE attach to the processor for detecting the received signal (paragraph 011) but is silent on teaching the detector is included in

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the processor. The appellant admitted prior art (figure 3) teaches a detector 307 integrated in a processor 100.

It would have been obvious to one of ordinary skill in the art to include the detector into the processor because this represents a cost saving by having fewer parts on the circuit board.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 in view of Twitchell Jr. US Patent Application Publication 20050215280 and further in view of Pratt et al. 20040198233.

Regarding claim 10, Kuttruff et al. teaches the detector generating a signal to the processor (paragraph 0039) but is silent on teaching the detector includes a frequency detector for detecting a variation in frequency interrupt port to the processor. Pratt et al. in an art related RFID device teaches a frequency detector for detecting the received frequency (paragraph 0048).

It would have been obvious to one of ordinary skill in the art for the detector to include a frequency detector for detecting a variation in frequency this allows the proper demodulating and decoding scheme to be used to capture the received data.

(10) Response to Argument

Appellant argues on page 11 that the reference of Kuttruff fails to disclose a memory portion for storing RFID data together with mobile terminal protocol data. It is the examiner's position that Kuttruff et al. teaches storing protocol data which represent criteria for changing

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over transmission and the RFID data for controlling the modulators, encoders, and decoders are stored in the EEPROM of the processing unit (paragraph 056). The reference of Kuttruff et al. also teaches the memory of the processing unit supplies the RFID data to be transmitted (paragraph 031) further suggesting that the RFID data is stored in the memory of the processing unit. The appellant use of the phrase "together with" is broad and therefore the storing of the RFID data and the protocol data in the memory of the processing unit meet the limitation of a memory portion for storing RFID data together with mobile terminal protocol data.

Appellant argues on page 12 that the reference of Kuttruff teaches away from a memory portion that stores RFID data together with mobile terminal protocol data. It is the examiner's position that Kuttruff et al. teaches storing protocol data in the memory of the processing unit (paragraph 056) and also teaches the memory of processing unit supplies the RFID data to be transmitted (paragraph 031) further suggesting that the RFID data is stored in the memory of the processing unit. The claims do not recite that a single memory element stores the claimed data, merely that a memory portion stores the data. It is the examiner's position that multiple memory elements can make up a memory portion as claimed.

Regarding appellant argument on pages 13-14 regarding the first and second clock generator, the reference of Ohkawa et al. is relied upon for teaching RFID device having a first clock generator (61) generating a clock to the processor (8) and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal generated by generator (62) is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a first and second clock for the receiver and

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transmission part of the RFID device (figure 2) and the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2). Appellant argument regarding the stability of clock as provided in the appellant invention is not claimed.

Appellant argues on page 13 that the reference of Ohkawa only teaches one clock as opposed to a second clock generator as recited in claim 14, it is the examiner's position that the reference of Ohkawa teaches a first clock generator (61) generating a clock to the processor (8) and the memory of the processor (figure 2) and a second clock generator (62) generating a clock to the modulator (figure 3).

Appellant argues that the teachings of Twitchell fail to teach a first clock generator and a second clock generator, it is the examiner's position that the reference of Twitchell is not relied on for teaching this limitation.

Appellant argues on pages 15-16 that the reference of Twitchell fail to teach or suggests the processor command the power block to provide electric power to the RFID module, it is the examiner's position that the reference of Twitchell is relied upon for teaching the use of a microprocessor to control power to a module (paragraph 065). The reference of Kuttruff et al. is relied upon for teaching a power block comprising rectifier and voltage regulator for supplying power to the RFID module illustrated in figure 2 and further described in paragraph 048. The reference of Ohkawa et al. also teaches the power block (4) connected to the first clock generator (61), the processor and RFID module (figure 2).

Appellant argues that the reference of Twitchell is not prior art, it is the examiner's position that the reference of Twitchell has a priority date of May 16, 2002, which precedes the appellant effective filing date of October 7, 2003.

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Regarding appellant argument regarding the lumping of the rejection of claims 6 and 7, the rejection of claims 6 and 7 are now separated.

Regarding appellant argument regarding the lumping of the rejection of claims 6-7 and 16-19 on pages 17-18, the rejection of these claims are now separated.

Regarding claims 6,7, 16-19, the appellant concludes that they have shown that there are missing features not taught by the references. The appellant fails to explain or point out what these features might be. This is not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

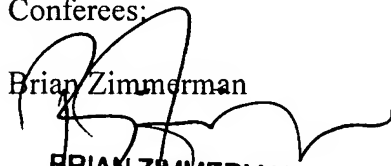
Respectfully submitted,

Vernal Brown

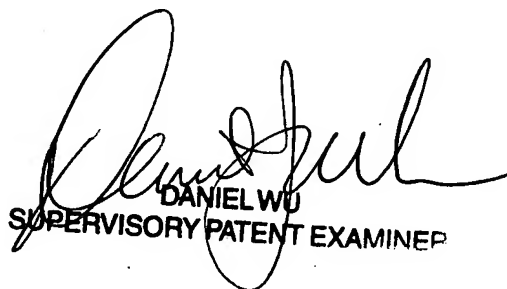


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